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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: **U-Ming Ko**

Docket: **TI-29632**

Serial No.: **09/723,563**

Examiner: **TBD**

Filed: **11/28/2000**

Art Unit: **TBD**

For: **Input/Output Architecture for Integrated Circuits**

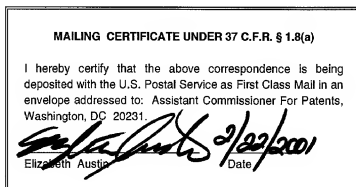
**TRANSMITTAL OF FORMAL DRAWINGS**

February 22, 2001

Assistant Commissioner For Patents

Attn: Official Drafts Person

Washington, DC 20231



Dear Sir:

Submitted herewith are 5 sheets of formal drawings.

Respectfully submitted,

*Ronald O. Neerings*

Texas Instruments Incorporated

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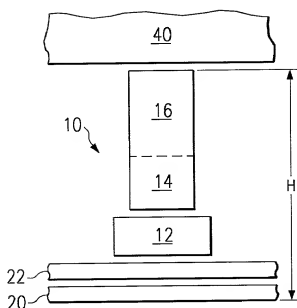
Reg. No.: 34,227

(972) 917-5299

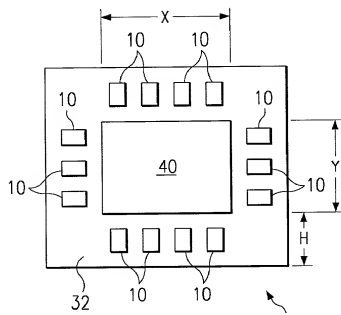
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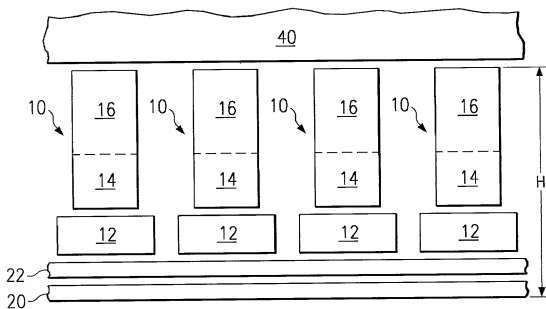
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*FIG. 1*  
(PRIOR ART)



*FIG. 2*  
(PRIOR ART)



*FIG. 3*  
(PRIOR ART)

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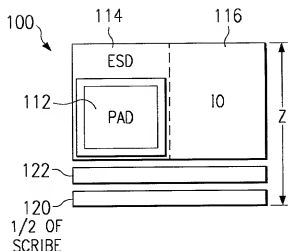


FIG. 4

FIG. 5

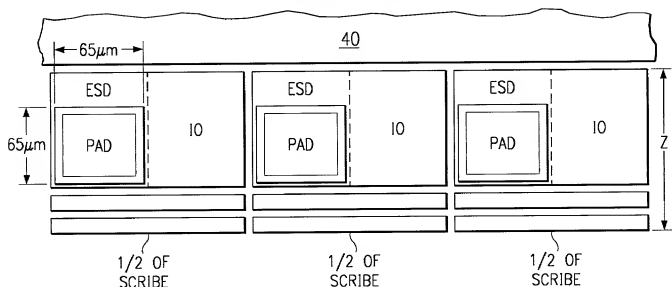
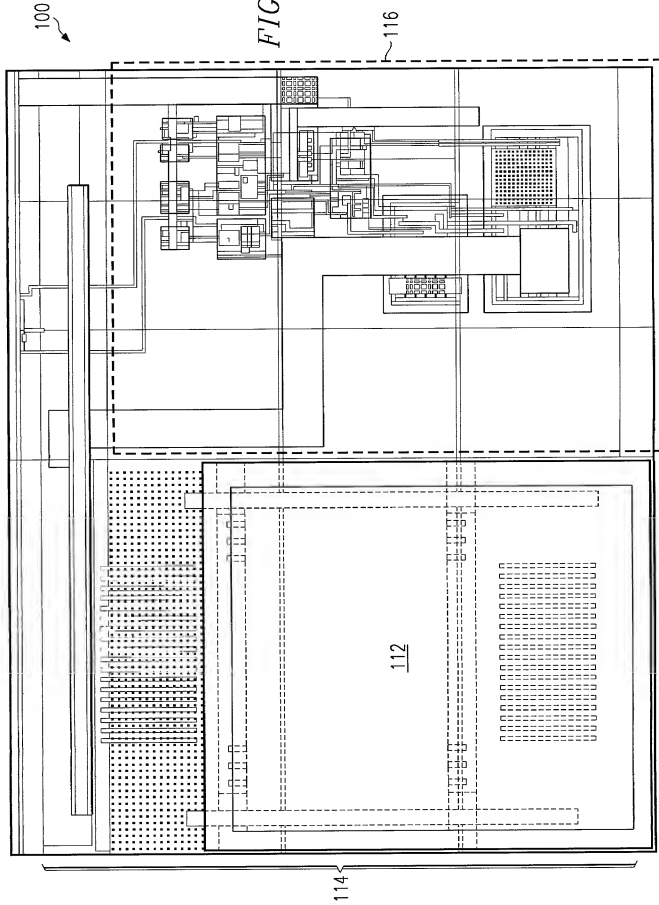


FIG. 6

CORE AREA, mm <sup>2</sup>	mm/SIDE	IO HEIGHT, μm	IO WIDTH, μm	AREA	MAX IO	WASTED AREA	% OF CORE
10	3.162278	H=188	75	12.51941	169	1.67	13%
		Z=120	108	11.57549	117		
20	4.472136	H=188	75	23.50442	239	2.33	10%
		Z=120	108	22.20423	166		
30	5.477226	H=188	75	34.26025	292	2.83	8%
		Z=120	108	32.68667	203		
40	6.324555	H=188	75	44.89744	337	3.26	7%
		Z=120	108	43.09339	234		
50	7.071068	H=188	75	55.45882	377	3.63	7%
		Z=120	108	53.45171	262		
60	7.745967	H=188	75	65.96634	413	3.97	6%
		Z=120	108	63.77566	287		

FIG. 7



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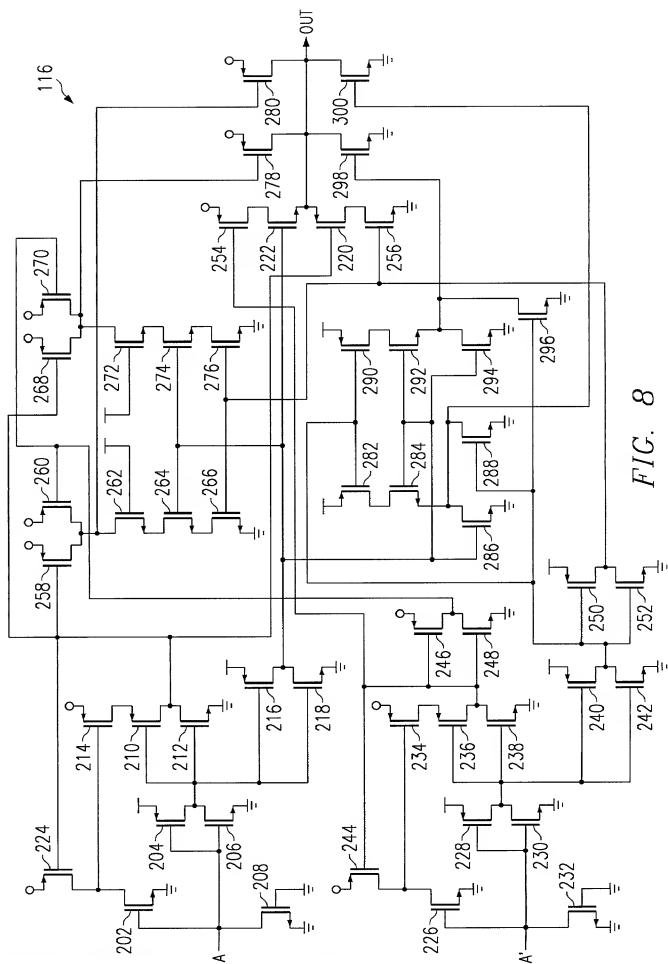


FIG. 8

FUNCTION	F0/SLEW	TYPE	TPLH	TPHL	TP	O/P SLEW
IV110	2SL/0.1ns	8-TRACK	0.2361	0.2143	0.2252	0.29935
		7-TRACK	0.2377	0.2192	0.22845	0.3033
	6SL/0.3ns	8-TRACK	0.4107	0.3535	0.3821	0.4479
		7-TRACK	0.4144	0.3605	0.38745	0.4545
NA210	2SL/0.1ns	8-TRACK	0.2718	0.2549	0.26335	0.3304
		7-TRACK	0.2697	0.2498	0.25975	0.3281
	6SL/0.3ns	8-TRACK	0.4526	0.4113	0.43195	0.493
		7-TRACK	0.4466	0.4027	0.42465	0.4883

FIG. 9